W129A

Custom Frequency Timing Generator

Features

- **Two clock outputs**
- **Cycle-to-cycle jitter absolute value less than 250 ps**
- **Supports 3.3V ±10% operation**
- **TTL compatible logic: V_{IL} = 0.8 Vmax, V_{IH} = 2.0 Vmin, V_{OL} = 0.4 Vmax, and V_{OH} = 2.4 Vmin**
- **OE and CTRL1 pins have internal pull-up**
- **CTRL2 and CTRL3 pins have internal pull-down**
- **45/55% duty cycle on all outputs**
- **25-Ohm output drivers**
- **Accepts 13.5-MHz input reference**
- **Built-in crystal oscillator circuit. The load presented to the crystal is 14 pF**

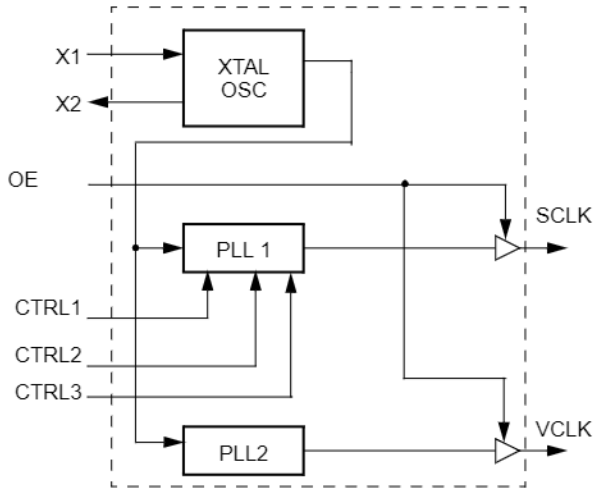
General Description

The W129A was designed to provide all the necessary timing signals for a home video game system. In order to facilitate passage of regulatory EMI testing, Cypress provides a range of options for its proprietary Spread Spectrum EMI reduction technique. Only the system clock utilizes the Spread Spectrum feature; the video clock runs at a steady frequency to ensure a high-quality picture.

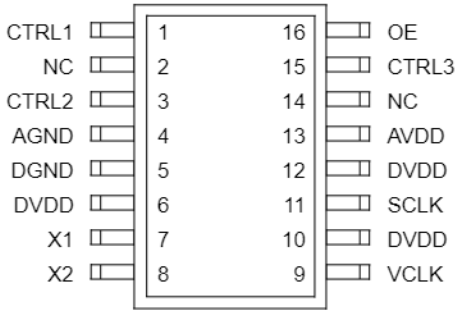
Table 1. Frequency Selection

CTRL3	CTRL2	CTRL1	OE	Spread%	SCLK (MHz)	VCLK (MHz)	PLL1 Ratio	PLL2 Ratio
0	0	0	1	–0.5%	33.333	54	200/81	4
0	0	1	1	±1.25%	33.333	54	200/81	4
0	1	0	1	–1.0%	33.333	54	200/81	4
0	1	1	1	±1.0%	33.333	54	200/81	4
1	0	0	1	–1.25%	33.333	54	200/81	4
1	0	1	1	±0.5%	33.333	54	200/81	4
1	1	0	1	–2.0%	33.333	54	200/81	4
1	1	1	1	±2.0%	36.7	54	106/39	4

Block Diagram



Pin Configuration



Functional Description

Clock Outputs

The W129A uses a unique clock output buffer design that minimizes system EMI and reduces clock ringing at the load. This is accomplished by "wave shaping" the clock output, which is used to produce an ideal clock signal waveform. This also eliminates the need for external dampening capacitors on the clock line. **The use of external clock output dampening capacitors is not recommended with the W129A.** For further information of clock output wave shaping, refer to Cypress Applications Brief AB-05.

The W129A output buffers are CMOS type which deliver a rail-to-rail (GND to V_{DD}) output voltage swing into a nominal capacitive load. Thus, output signaling is both TLL and CMOS level compatible. Nominal output buffer impedance is 25Ω.

PLL Circuits

The W129A PLL (phase-locked loop) circuits exhibit fast loop response. Output frequencies are stable within 3 ms after power-up. Upon changing the condition of CTRL1:3, the new SCLK clock frequency will stabilize within 1 ms.

The PLL circuits are optimized for low jitter, stable operation suitable for various processor applications. Compared to more traditional designs, these PLLs are less sensitive to power supply noise created by other system components or by the output buffers. On-chip PLL loop components further assure system noise rejection.

Crystal Oscillator

The W129A requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is $V_{DD}/2$.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W129A incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is 14 pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 14 pF should be used. This will typically yield reference frequency accuracies within ±100 ppm. To achieve similar accuracies with a crystal calling for a greater load, external capacitors must be added such that the total load (internal, external, and parasitic capacitors) equals that called for by the crystal. For example, the use of a crystal calling for a 20-pF load capacitance would require the addition of a 12-pF capacitor at both pins X1 and X2, each terminated to ground (viewed by the crystal, these external load capacitors are connected in series through the common ground). Failure to match capacitance or the use of a serial resonant crystal could result in an oscillator frequency error as high as 500 ppm.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CTRL1:3	1, 3, 15	I	***System Clock Control Inputs***: These three inputs control the frequency of the output and the bandwidth over which the output is spread.
VCLK	9	O	***Video Clock Output***: Provides a 54-MHz clock signal. This signal is not affected by inputs CTRL1:3.
SCLK	11	O	***System Clock Output***: Provides an output with frequency as specified in *Table 1*.
OE	16	I	***Output Enable***: When LOW, this input signal disables the System and Video Clock outputs.
NC	2, 14	NC	***No Connections***: Leave these pins unconnected (floating).
X1	7	I	***Crystal Connection or External Reference Frequency Input***: This pin has dual functions. It can be used as an external 13.5-MHz crystal connection or as an external reference frequency input.
X2	8	I	***Crystal Connection***: An input connection for an external 13.5-MHz crystal. If using an external reference, this pin must be left unconnected.
DVDD	6, 10, 12	P	***Digital Power Supply Connections***: Connect to 3.3V. Each DVDD pin should have a decoupling capacitor (such as 0.1 µF) placed as close to the pin as possible.
AVDD	13	P	***Analog Power Supply Connection***: Connect to 3.3V or 5.0V. This pin should have a decoupling capacitor (such as 0.1 µF) placed as close to the pin as possible.
DGND, AGND	5,4	G	***Ground Connections***: Connect all ground pins to the common system ground plane.

Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

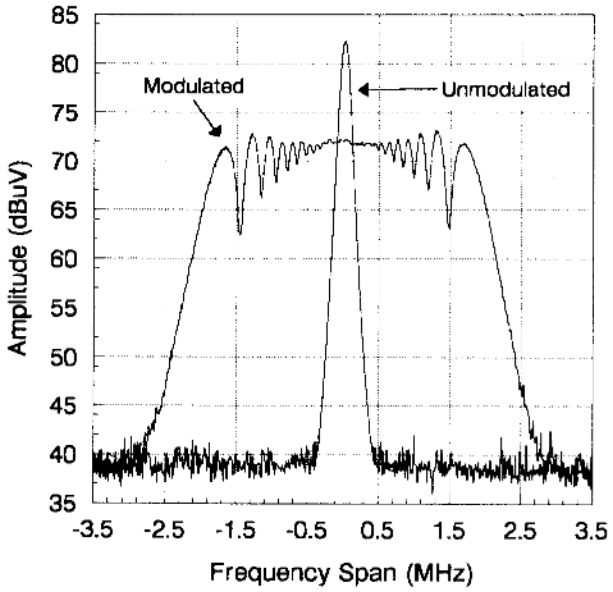


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

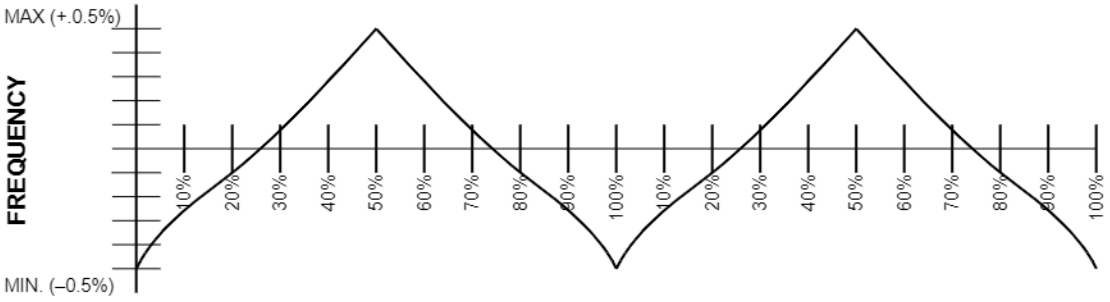


Figure 2. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on Any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C

DC Electrical Characteristics at 3.3V: T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			150	180	mA
V_{IL}	Input Low Voltage	V_{DD} = 3.3V			0.8	V
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{DD} = 3.3V	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V, includes pull-up			–30	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			10	µA
R_P	Input Pull-up Resistor	V_{IN} = 0V		500		kΩ
C_I	Input Capacitance	Except X1 and X2			6	pF
L_I	Input Inductance	Except X1 and X2			7	nH
C_L	XTAL Load Capacitance	Total load to crystal	10	12	14	pF

AC Electrical Characteristics: 0°C < T_A < 70°C, V_{DD} = 3.3V ± 10%[1]

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
t_{JC}	Output Clock Jitter, Cycle-to-Cycle	Note 3		±175	±250	ps
Z_O	Output Buffer Impedance			25		W
d_T	Output Duty Cycle		45.0	50.0	55.0	%
t_R	Rise Time	Between 0.4V and 2.4V	1.0	1.5	4.0	V/ns
t_F	Fall Time	Between 2.4V and 0.4V	1.0	1.5	4.0	V/ns
t_{PU}	Stabilization Time from Power-Up	To within 0.1% of final frequency		1.5	3.0	ms
f_A	Long Term Output Frequency Stability[2]	Over V_{DD} and T_A range			0.01	%

Notes:

1. All AC tests are performed using 22-pF lumped load. Measurements are taken at the load. Threshold voltage for timing measurements is 1.5V.
2. Long Term Output Frequency Stability is solely affected by crystal oscillator frequency shift.
3. Cycle-to-cycle jitter absolute value less than 250 ps.

Applications Information

Power Supply Connections

The major considerations can be summarized as follows:

1. Decoupling Capacitor - A 0.1-µF decoupling cap should be used for each VDD pin to minimize crosstalk between output frequencies. The trace to the VDD pin and to the ground via should be as short as possible.
2. Ferrite Bead (FB) - A common supply connection should be used for all W129A VDD pins. A ferrite bead should be used on this common supply to remove high-frequency system noise.
3. 22-µF Supply Filter Capacitor - The 22-µF capacitor filters low-frequency supply noise that may produce clock output jitter. Depending on the particular motherboard, this capacitor may not be required; its use should be considered optional. Mounting pads should be implemented in PCB layout. Use of this capacitor in production should be determined upon prototype evaluation.
4. PCB power supply traces should be at least 20 mils wide to assure adequate trace impedance.

Ground Connections

All ground connections should be made to the main system ground plane. These connections should be as short as possible. No cuts should be made in the ground plane around the clock device since this can increase system EMI and reduce clock performance.

Clock Output Lines

Short Clock Lines

Clock lines shorter than one inch may be connected directly from the clock output to the clock load; no series resistor is needed on the clock line. This is because short clock lines do not behave like a transmission line and therefore termination matching is not required.

Long Clock Lines

Clock lines longer than one inch must be treated as a transmission line to achieve good clock performance at the load and to minimize system EMI. There are three clock transmission line configurations generally acceptable for use with the W129A.

1. Point-to-Point Clock Line—The clock output drives only one clock load as shown in *Figure 3*.
2. Modified Point-to-Point Driving Two Loads—This method is used to drive two clock loads that are close to each other. Short stubs are used at the end of the clock line to divide the clock signal as shown in *Figure 4*.
3. Split Clock Line Driving Two Loads—This method is used to drive two clock loads that are not near each other. It is important that each leg of the branch is approximately the same length (no more than one inch difference in length). Each clock line has its own series termination resistor as shown in *Figure 5*.

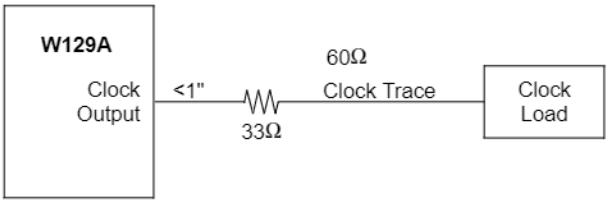


Figure 3. Point-to-Point Clock Line

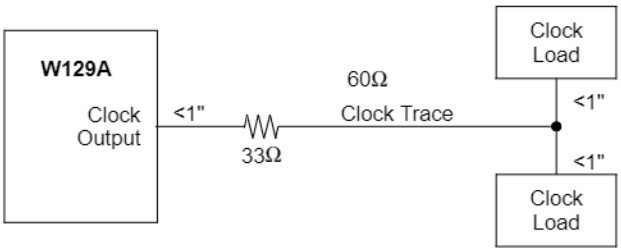


Figure 4. Modified Point-to-Point Driving Two Loads

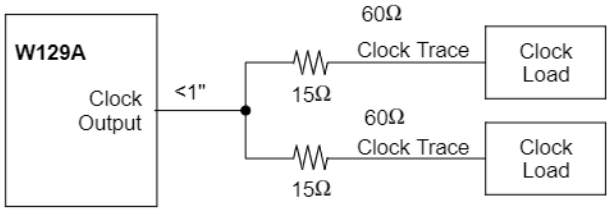


Figure 5. Split Clock Line Driving Two Loads

Additional points to consider when implementing long clock lines:

1. The series termination resistor (sometimes called “damping resistor”) must be placed in series with the clock line as close to the clock output as possible (within one inch).
2. A clock line load capacitor need NOT be used with the W129A. Because of Cypress’s wave-shaped clock output, the load capacitor is not needed. Use of a load capacitor on the output clock may result in excessive clock rise and fall time. (A clock output load capacitor is sometimes suggested by other clock companies to control EMI. The circuit board may include a location for this load capacitor, but the capacitor should not be loaded when using the W129A. When an output load capacitor is used, it is normally connected to the clock line just following the series termination resistor and terminated to ground. When used with a clock device from another company, it can help control output ringing and EMI caused by the rapid rise/fall rates produced by these clock devices.)
3. Avoid using vias in clock line. If absolutely required, place vias near source or termination end of line.

4. Increase space between clock lines and other high speed digital lines.
5. Do not run clock traces underneath clock device, crystal, or crystal connection traces.

Logic Inputs

Logic inputs CTRL1:3 and OE can be tied directly to ground to select a "0" input or directly to V_{DD} to select a "1" input. Logic inputs CTRL1 and OE include internal low current pull-up devices, so an unconnected input will assume a logic "1" condition. Logic inputs CTRL2 and CTRL3 include internal pull-down devices. However, the internal pull-up/down devices may not be dependable when using long traces on the input pins. When using a long input trace, an external 10K ohm pull-up resistor should be connected to the input line (anywhere on the line) if the input line could be left floating. The pull-up resistor is connected between the input trace and V_{DD}.

Summary of PCB Layout Tips

1. Keep the crystal close to the X1, X2 pins.
2. Do not run any clock output or signal traces underneath the clock device, crystal, or crystal connection traces.
3. The power supply and ground traces to the pins must be kept wide; it should be at least 20 mils wide.
4. Place VDD decoupling capacitors close to VDD pins.
5. Place clock line termination resistors close to clock outputs.
6. Try to minimize use of clock via's. If they are needed, put at the beginning or end of the clock line.
7. Do not locate the W129A close to other high-speed digital chips.
8. Use an external 10-kΩ pull-up resistor on long input traces if they are floated.

Recommended PCB Components

Listed below are examples of components that can be used to support the W129A.

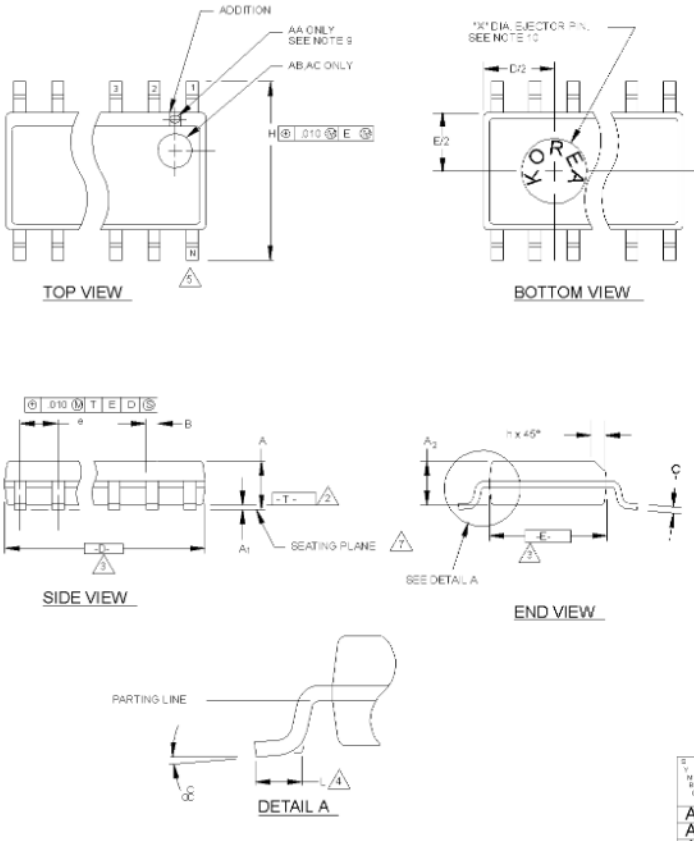
- FB (Ferrite Bead)
  - Fair-Rite Part# 2743019447
    3 µH, 5A working current
    Surface mount package
- C1 (Filter Capacitor)
  - AVX Part# TAJC226K016R
    22 µF, W16 VDC
    Tantalum
    Surface mount package
- Decoupling Capacitors
  - muRata Part# GRM39Y5V104Z016AD
    0.1 µf, 16WVDC
    Surface mount, EIA size 0603
- Series Termination Resistor
  - EIA size 805 (1/10 watt)

Ordering Information

Ordering Code	Package Name	Package Type
W129A	G	16-Pin SOIC (150-mil)

Package Diagram

16-Pin Small Outline Integrated Circuit, Narrow (SOIC, 0.150 Inch)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	3			5
	MIN.	NOM.	MAX.	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.061	.064	.068	AA	.189	.194	.196	8
A_1	.004	.006	.0098	AB	.337	.342	.344	14
A_2	.055	.058	.061	AC	.386	.391	.393	16
B	.0138	.016	.0192					
C	.0075	.008	.0098					
D	SEE VARIATIONS			3				
E	.150	.155	.157					
e	.050 BSC							
H	.230	.236	.244					
h	.010	.013	.016					
L	.016	.025	.035					
N	SEE VARIATIONS			5				
∝	0°	5°	8°					
X	.085	.093	.100					

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	3			5
	MIN.	NOM.	MAX.	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.55	1.63	1.73	AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25	AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55	AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49					
C	0.19	0.20	0.25					
D	SEE VARIATIONS			3				
E	3.81	3.94	3.99					
e	1.27 BSC							
H	5.84	5.99	6.20					
h	0.25	0.33	0.41					
L	0.41	0.64	0.89					
N	SEE VARIATIONS			5				
∝	0°	5°	8°					
X	2.16	2.36	2.54					

Revision History

Document Title: W129A Custom Frequency Timing Generator Document Number: 38-07276				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110864	11/15/01	IKA	Converted to Cypress format from IC Works format
*A	113092	04/03/02	IKL	Changes to title and overview (remove reference to Sega)